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Sheet 1 of 1

FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 856063.547D1	APPLICATION NO.
INFORMATION DISCLOSURE STATEMENT *(Use several sheets if necessary)*		APPLICANTS Salvatore Lombardo et al.	
		FILING DATE July 7, 2003	GROUP ART UNIT

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
AS	AA	4,343,080	08/10/82	Hataishi et al.	29	571	
	AB	5,028,557	07/02/91	Tsai et al.	437	59	
	AC	5,126,278	06/30/92	Kodaira	437	24	
	AD	5,635,423	06/03/97	Huang et al.	437	195	
	AE	5,659,201	08/19/97	Wolleson	257	758	
	AF	5,712,177	01/17/98	Kaushik et al.	437	42	
	AG	5,753,967	05/19/98	Lin	257	635	
	AH	5,643,825	07/01/97	Gardner et al.	437	70	
	AI	5,814,555	09/29/98	Bandyopadhyay et al.	438	619	
	AJ	5,821,149	10/13/98	Schuppen et al.	438	312	
	AK	5,847,460	12/08/98	Liou et al.	257	751	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
AS	AL	03-292740	12/24/91	Japan		
AS	AM	0697716A2	02/21/96	EP		
	AN					

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

AS	AO		S. Wolf et al., "Silicon Processing for the VLSI Era V1" - *Process Technology*, 1986, pp 182-183.
	AP		Gomi et al., "A Sub-30psec Si Bipolar LSI Technology," in International Electron Devices Meeting, San Francisco, December 11-14, 1988, *Institute of Electrical and Electronics Engineers*, No. 1988, pp 744-747, 1988.
	AQ		Lombardo, S. et al., "Ge Ion Implantation in Si for the Fabrication of Si/Ge Si Heterojunction Transistors," *Materials Chemistry and Physics, 46*(2-3), pp. 156-160, 1996.

EXAMINER	DATE CONSIDERED
AJ	11/5/04

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).